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A Study Of Alternative Topologies For Network-On-Chip Architectures

Deepika Pandey[*1], Priyanka Sahu[2], Anurag Punde[3]
*1Acropolis Institute of Technology & Research, Indore
[2]Central India Institute of Technology, Indore (M.P.), India
deepsadream@gmail.com

Abstract

With increase in complexity of system on chip and many components are incorporated in it, the conventional interconnection is unable to fulfill the demands. The massive load on the network reduces the efficiency and effectiveness. Selection of better topology provides lesser complexity in the network, lesser power consumption and increases the throughput of the network. In this paper we have proposed the new approach i.e. Network on Chip that overcomes the above problem by providing the better solution. The main concern of NoC is that, it targets specially the infrastructure and focuses upon the optimized design topology.

Keyword: Soc, NoC, Mesh topology.

I. Introduction

With the technological development in the field of integrated circuits has facilitated the designer to accommodate billions of transistors. Traditionally, ICs have been designed with dedicated point-to-point connections, with one wire dedicated to each signal. For large designs, in particular, this has several limitations from a physical design viewpoint. The wires occupy much of the area of the chip, and in nanometre CMOS technology, interconnects dominate both performance and dynamic power dissipation, as signal propagation in wires across the chip requires multiple clock cycles. The exponential decrease in the size has facilitate integration of heterogeneous IP cores in to the single chip leading the new era of integrated circuits called System-on-Chip. It is the technology that packages all the necessary electronic circuits and part for the system. However, with the increase of number of components, the performance, efficiency, power and communication infrastructure is now gaining equal importance. The traditional approaches of connecting these heterogeneous IP cores are not actually accomplishing the demand for these very complexes Structures. Furthermore, the connection between the different nodes causes the problems like synchronization, packet lost, delay, and more power consumption and also increases the load.

[1] Traditional bus and crossbar based methods to communicate become very incompetent, resulting massive number of links and also increases the congestion on the network. The network on chip approaches promises the alternative to traditional bus based and point to point communication. Network-on-Chip or Network-on-a-Chip is an approach to designing the communication subsystem between IP cores in a System-on-a-Chip (SoC). NoCs can span synchronous and asynchronous clock domains or use unclocked asynchronous logic. NoC applies networking theory and methods to on-chip communication and brings notable Improvements over conventional bus and crossbar interconnections. NoC improves the scalability of SoCs, and the power efficiency of complex SoCs compared to other designs. The SoCs consists of heterogeneous IP-Cores such as processors; memory blocks and it may also contain anolog, digital and mixed signals. Each of these cores connected with NoCs through a network interface or network adopter module. The NoCs contains the network of routers from end to end delivery of the packets from IP Cores. The network interface provides flawless integration of these IP Cores and network.

The design space of the NoCs is very large and includes topology selection (Mesh, Star, etc.), circuit switch, packet switch and other parameters (link width, frequency, etc.)[4]. NoC links can reduce the complexity of designing wires for predictable speed, power, noise, reliability, etc., thanks to their regular, well controlled structure. From a

system design viewpoint, with the advent of multi-core processor systems, a network is a natural architectural choice.

A NoC can provide separation between computation and communication, support modularity and IP reuse via standard interfaces, handle synchronizations issues, serve as a platform for system test and hence the engineering productivity. A NoCs buffers and links can consume near 75% of the total NoC power [5], thus there is a significant benefits to optimising buffer size, link length and bandwidth of NoCs design.

II. Survey

Network-on-Chip (NoC) is an emerging paradigm using packet switched networks for communications within large VLSI system-on-Chip. NoCs are poised to provide enhanced performance, scalability, modularity, and design productivity as compared with previous communication architectures such as busses and dedicated signal wires. With the emergence of large number of cores in general purpose and system-on-chip (SoC), NoCs are likely to be prevailing on-chip interconnect fabric. [6]

The early work and basic principles of NoC paradigm were outlined in various seminal articles, for example [7-17] and few text books [18-20]. However, the aforementioned sources do not present many implementation examples or conclusions. Networking concepts from the domains of telecommunication and parallel computer do not apply directly on chip. From a networking perspective, they require adaptation because of the unique nature of VLSI constraints and cost e.g. Area and power minimization are essential; buffer space in on-chip switches are limited, latency is very important, etc. At the same time, there are new degrees of freedom available to the network designer, such as the ability to modify the placement of network endpoints. From the view point of VLSI designer, many well understood problems in the real aim of chip development methodology get a new slant when they are formulated for a NoC based system, a new trade-offs need to be comprehended. Therefore, the field offer opportunities for noble solutions in network engineering as well as system architecture, circuit technology, and design automation. [6]

Current complex on-chip systems are also modular, but most often the modules are interconnected by an on-chip bus. The bus is a communication solution inherited from the design of large board- or rack-systems in the 1990's. It has been adapted to the SoC specifics and currently several widely adopted on- chip bus specifications are available [31-34].

While the bus facilitates modularity by defining a standard interface, it has major disadvantages. Firstly, a bus does not structure the global wires and does not keep them short. Bus wires may span the entire chip area and to meet constraints like area and speed the bus layout has to be customized [35]. Long wires also make buses inefficient from an energy point of view [36]. Secondly, a bus offers poor scalability. Increasing the number of modules on-chip only increases the communication demands, but the bus bandwidth stays the same. Therefore, as the systems grow in size with the technology, the bus will become a system bottleneck because of its limited bandwidth. Recently, network-on-chip (NoC) architectures are emerging as a candidate for the highly scalable, reliable, and modular on- chip communication infrastructure platform [11]. The NoC architecture uses layered protocols and packet-switched networks which consist of on-chip routers, links, and network interfaces on a predefined topology. There have been many architectural and theoretical studies on NoCs such as design Methodology [10], [11], topology exploration [21], Quality-of- Service (QoS) guarantee [22], resource management by software [23], and test and verifications [24].

In large-scale SoCs, the power consumption on the communication infrastructure should be minimized for reliable, feasible, and cost-efficient implementations. However, little research has reported on energy- and power-efficient NoCs at a circuit or implementation level, since most of previous works have taken a top-down approach and they did not touch the issues on a physical level, still staying in a high-level analysis. Although a few of them were implemented and verified on the silicon [25], [26],they were only focusing on performance and scalability issues rather than the power-efficiency, which is one of the most crucial issues for the practical application to SoC design.

Network-on-Chip (NoC) architectures employing packet-based communication are being increasingly adopted in

System-on- Chip (SoC) designs. In addition to providing high performance, the fault-tolerance and reliability of these networks is becoming a critical issue due to several artifacts of deep sub-micron technologies. Consequently, it is important for a designer to have access to fast methods for evaluating the performance, reliability, and energy-efficiency of an on-chip network. [27] While on-chip networks have been proposed and studied in the academic literature, to date there have been very few implementations of routed on-chip networks. Dally and Towels [10] proposed a 2D torus network as a replacement for global interconnect. They claim that on-chip network modularity would shorten the design time and reduce the wire routing complexity. On-Chip routed networks have also been proposed for use in SoCs such as in CLICHÉ [12], in which a 2D mesh network is proposed to interconnect a heterogeneous array of IP blocks.

A performance analysis also shows that dynamic resource allocation leads to the lowest network latencies, while static allocation may be used to meet QoS goals. Combining the power and performance figures then allows an energy-latency product to be calculated to judge the efficiency of each of the network [28].

In his work, Nikolay K. Kavaldjiev, used run-time reconfigurable NoC for streaming DSP applications taking the advantage of a global communication architecture that avoids limitation by structuring and shortening the global wires. He also proposed architecture of a virtual channel router, which in contrast to conventional architectures is able to provide predictable communication services and has a lower implementation area and cost than conventional architectures. Dynamic reconfiguration is essential to support the dynamically changing demands of the application domain: the system operates in a constantly changing environment. The user demands change (e.g., starting/terminating applications), the environmental conditions change (e.g., available networks, wireless channel conditions) and the available power budget also changes (decreasing battery budget or connected to the mains). The set of running applications and tasks in the system adapts dynamically to these changes. The run-time eexploring Alternative Topologies for Network-on-Chip Architectures reconfiguration modifies the system communication demands. For example, a new data stream may be needed or some of the old streams may be redirected or replaced. The NoC must be able to handle such dynamically changing traffic conditions. Run-time changes in part of the traffic must be possible without disturbing the rest of the traffic. The network reconfiguration time must be short enough to enable adequate system reaction time and reconfiguration must be transparent to the user. [30] The major goal of communication-centric design and NoC paradigm is to achieve greater design productivity and performancebyhandling the increasing parallelism, manufacturing complexity, wiring problems, and reliability. The three critical challenges for NoC according to Owens et al. are: power, latency, and CAD compatibility [17]. The key research areas in Network-on-Chip design can be summarized as [29]:

Communication infrastructure: topology and link optimization, buffer sizing, floor planning, clock domains, power
Communication paradigm: routing, switching, flow control, quality of service, network interfaces benchmarking and traffic characterization for design and runtime optimization Application mapping: task mapping/ scheduling and IP component mapping.

III. Methodology

Network-on-Chip is a new paradigm for interconnecting today's heterogeneous IP cores based System-on-Chips (SoCs). In SoC's IP Cores are connected to network of routers using network interfaces and network is used for packet switched on- chip communication. Conventional computer design tools i.e. Packet Tracer 5.3 utility from CISCO are used for network design and simulation. It provides a versatile practice and visualization environment for the design, configuration, and troubleshooting of network environments. The work done by us uses same tool to compare two topologies. The 2-D mesh is currently the most popular regular topology used for on-chip networks in tile-based architectures, because it perfectly matches the 2-D silicon surface and is easy to implement. However, a number of limitations have been proved in the open literature, especially for long distance traffic. In this type of topology, every node has a dedicated point to point link to every other node in the network. This means each link carries traffic only between the two nodes it connects.

If N is total no of nodes in network. Number of links to

Connect these nodes in mesh = N (N-1)/2 each node should have (N-1) I/O ports as it require connection to every another node.

The advantages are:

- No traffic problem as there are dedicated links. Robust as failure of one link does not affect the entire system.
- Security as data travels along a dedicated line.
- Points to point links make fault identification easy. The disadvantages are:

The hardware is expansive as there is dedicated link for any two nodes and each device should have (N-1) I/O ports. There is mesh of wiring which can be difficult to Manage Installation is complex as each node is connected to every node.

As earlier studies have shown that maximum power is consumed by links and interconnect infrastructure. Reducing interconnects and links will result in lower power consumption but can also affect the performance and reliability negatively. The topology suggested by us reduces the number of links thus resulting into lower power consumption keeping same level of reliability and performance levels.

IV. Conclusion

The results achieved in terms of time and reduction in number of links displayed here is encouraging and motivates us to take the work further. As discussed earlier the NoC technology can borrow the tools and techniques from conventional computer network technology with required customization. In our future work, we intend to test same on a standard NoC benchmark. The other design parameters on NoC will also be explored.

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